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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/236,526	01/25/1999	FELIX KHOURI	081862.P119	1370

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EXAMINER	
TSEGAYE, SABA	
ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 06/20/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/236,526	KHOURI ET AL.	
	Examiner	Art Unit	
	Saba Tsegaye	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9-14,16 and 18-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,9-14,16 and 18-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1-5, 7, 9-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rakavy in view of Ozaki (US 6,124,802).

Regarding claims 1, 9 and 10, Rakavy discloses, in Fig. 4, a method of managing a network switch having a processor card including a memory and a processing unit in the processor card comprising:

detecting an error (step 438);

determining if the error is ignorable (step 437);

performing a hitless rebuild in the processor card (steps 437, 417, 418).

Rakavy fails to show the step of determining whether the number of hitless rebuilds has exceeded a pre-given threshold and if the error is determined to be ignorable and threshold has not been reached.

Note that to start or reset a processor after error detected is well known in computer and multi-processor systems.

Ozaki teaches "determining whether a threshold has been reached" and performing a re-initialization/rebuild in the processor card when the threshold is reached (column 6, line 47-column 7, line 10). Neither reference explicitly states that the rebuild should occur if the error is determined to be ignorable and threshold has not been reached. However, as is known in the art, the software in the processing unit cloud be modified to perform in this manner since the threshold and type of error are known.

It would have been obvious to one skilled in the art at the time the invention was made to add a threshold determination method, such as that suggested by Ozaki, in the Rakavy system. Doing so would provide a fault tolerant system that more effectively recognizes and handles recoverable faults and reduce the amount of service disruptions for devices connected to the switch nodes.

Regarding claims 2 and 11, Rakavy discloses, in Fig 4., the method wherein the hitless rebuild includes:

performing an initialization of the memory (step 417); and

protecting a portion of the memory from access by the processing unit during the initialization (column 6, line 63-column 7, line 1).

Regarding claims 3 and 12, Rakavy discloses the method wherein the performing of the hitless rebuild further comprises protecting a portion of the memory that contains a set of routing tables (column 15, lines 3-39).

Regarding claims 4 and 13, Rakavy discloses the method wherein the performing of the hitless rebuild further comprises protecting a portion of the memory that contains a set of state tables (column 15, lines 3-39).

Regarding claims 5 and 14, Rakavy discloses the method wherein the memory is accessed through a set of memory addresses and the performing of a hitless rebuild further

comprises preventing the processing unit from accessing a predetermined set of memory addresses in the set of memory addresses (column 2, lines 43-52).

Regarding claims 7 and 16, Rakavy discloses the method further comprising setting the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached (Fig. 4, steps 437, 435, 436).

Rakavy fails to show the step of determining whether threshold has been reached. However, as is known in the art, the software in the processing unit could be modified to perform in this manner since the threshold within an amount of time is known.

It would have been obvious to one skilled in the art at the time the invention was made to add a threshold determination method in the Rakavy system to reduce the amount of rest and service disruption of devices in the communication system.

2. Claims 18, 23, 28, 33, 38, 44, 50 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art (pages 1-4) in view or Klecka et al. (US 6,393,582).

The Admitted prior art discloses a network switch having a processor card including a memory, a stats table, and a routing table that contains the list of current connections. Further, the Admitted prior art discloses reinitializing software, in response to an error that is executed on a networking device card.

However, the Admitted prior art does not expressly disclose a memory that stores information that can be used by the processor to execute the software and reinitializing not deleting the state table information from the memory.

Klecka teaches fault tolerant data processing architecture, more particularly to a reset and re-initialization process in the face of a divergence, i.e., saving state to memory (claimed reinitializing not deleting the state table information from the memory), resetting the processor units, and restarting them from the prior saved processor state (column 7, lines 26-46; column 8, lines 35- 49).

It would have been obvious to one ordinary skill in the art at the time of the invention was made to store information that can be used by the processor to execute the software and reinitializing not deleting the state table information from the memory, such as that suggested by Klecka, in the memory of the Admitted prior art in order to provide a system that quickly and smoothly recover from the detected error (column 2, lines 12-30).

3. Claims 19-21, 24-26, 29-31, 34-36, 39-42, 45-48, 51-53 and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Klecka as applied to claims 18, 23, 28, 33, 38, 44,50, and 55 above, and further in view of Rakavy et al. (US 6,324,644).

The Admitted prior art in view or Klecka discloses all the claim limitations as stated above except for non-volatile memory, volatile memory, and random access memory.

Rakavy teaches, in Fig. 2, a non-volatile memory 125, volatile memory and random access memory 120. Further, Rakavy teaches that the non-volatile memory does not change state when the computer is reset.

It would have been obvious to one ordinary skill in the art at the time of the invention was made to add non-volatile memory, volatile memory, and random access memory, such as

that suggested by Rakavy, in the memory of the Admitted prior art in view or Klecka in order to provide a memory that shared by another program or by an interrupt service routine.

4. Claims 22, 27, 32, 37, 43, 49, 54 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Klecka as applied to claims 18, 23, 28, 33, 38, 44,50, and 55 above, and further in view of Treu (US 5,245,615).

The Admitted prior art in view of Klecka discloses all the claim limitation as stated above except for dynamic random access memory.

Note that dynamic random access memories are more commonly used than RAMs because dynamic random memory is less expensive than static RAM and their circuitry is simpler.

True teaches that random access memory comprises dynamic random access memory (column 2, lines 65-67).

It would have been obvious to one ordinary skill in the art at the time the invention was made to use dynamic RAM, such as that suggested by True, in the memory of the Admitted prior art in view of Klecka in order to provide less expensive memory.

Response to Arguments

5. Applicant's arguments with respect to claims 1-5, 7, 9-14, 16 and 18-59 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (703) 308-4754. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.

ST
June 13, 2003

JOHN PEZZLO
PRIMARY EXAMINER